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FIG. 1
Prior Art

100

State	L0	L1	L2	L3	State	L0	L1	L2	L3
1	0	0	0	0	9	0	0	0	1
2	1	0	0	0	10	1	0	0	1
3	0	1	0	0	11	0	1	0	1
4	1	1	0	0	12	1	1	0	1
5	0	0	1	0	13	0	0	1	1
6	1	0	1	0	14	1	0	1	1
7	0	1	1	0	15	0	1	1	1
8	1	1	1	0	16	1	1	1	1



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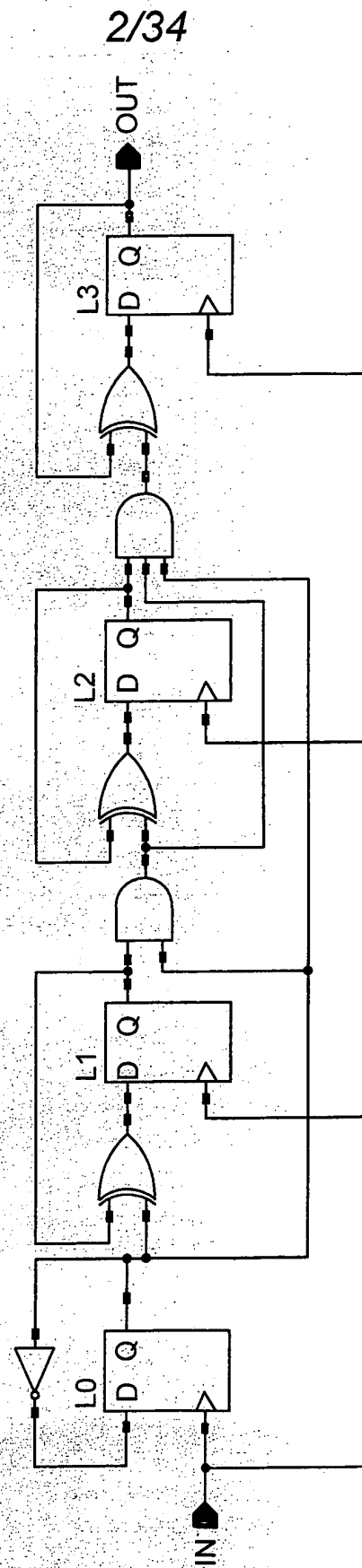
FIG. 1
Prior Art

100

State	L0	L1	L2	L3	State	L0	L1	L2	L3
1	0	0	0	0	9	0	0	0	1
2	1	0	0	0	10	1	0	0	1
3	0	1	0	0	11	0	1	0	1
4	1	1	0	0	12	1	1	0	1
5	0	0	1	0	13	0	0	1	1
6	1	0	1	0	14	1	0	1	1
7	0	1	1	0	15	0	1	1	1
8	1	1	1	0	16	1	1	1	1

FIG. 2
Prior Art

101



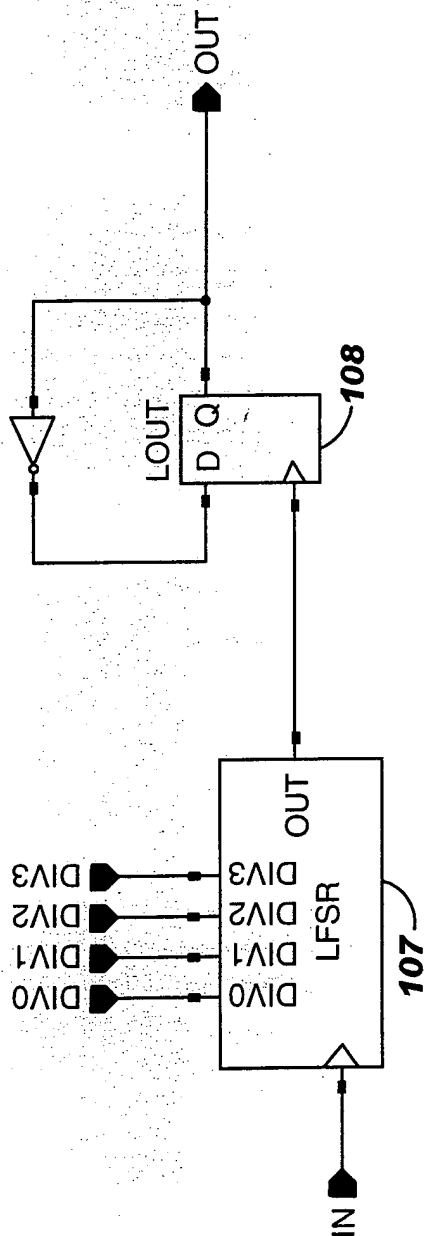
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FIG. 6
Prior Art**106**

State	L0	L1	L2	L3	State	L0	L1	L2	L3
1	0	0	0	1	9	0	1	0	1
2	1	0	0	0	10	1	0	1	0
3	0	1	0	0	11	1	1	0	1
4	0	0	1	0	12	1	1	1	0
5	1	0	0	1	13	1	1	1	1
6	1	1	0	0	14	0	1	1	1
7	0	1	1	0	15	0	0	1	1
8	1	0	1	1					

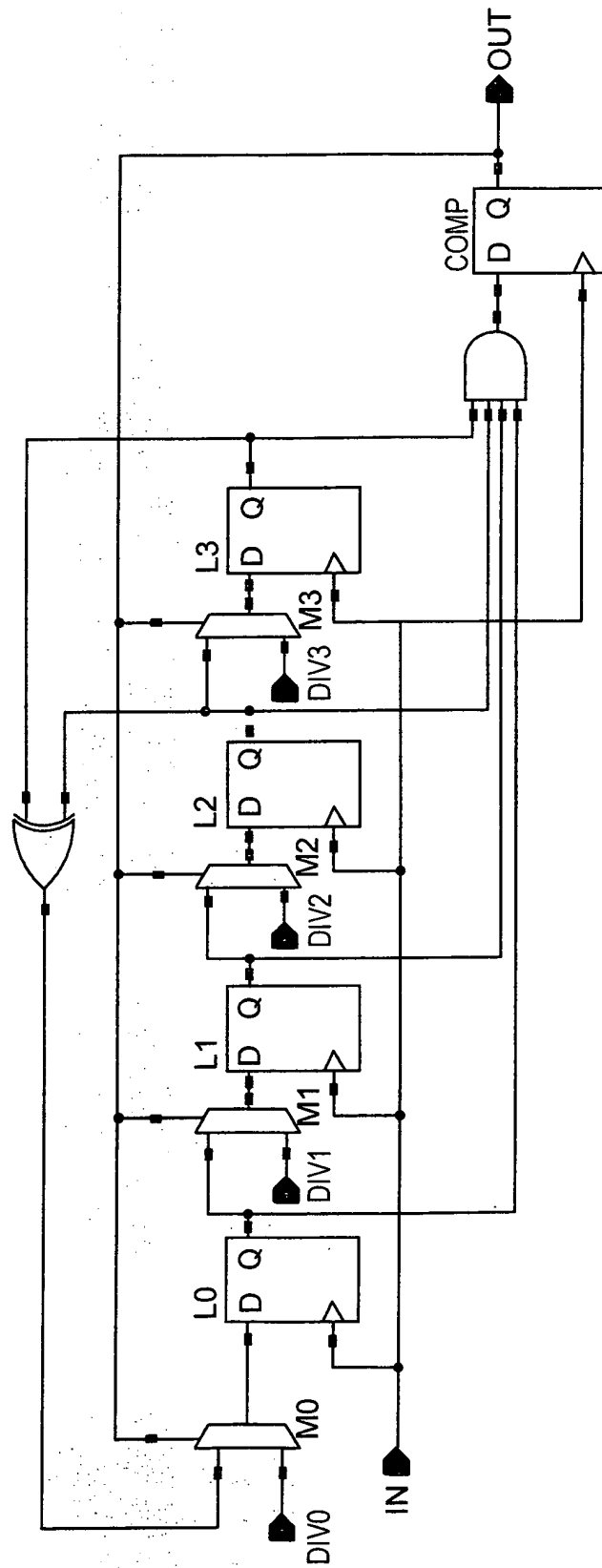
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FIG. 7



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FIG. 8



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FIG. 9

LFSR Divide Value	DIV0	DIV1	DIV2	DIV3	LFSR Divide Value	DIV0	DIV1	DIV2	DIV3
1	0	0	0	0	9	1	1	0	0
2	1	1	1	1	10	1	0	0	1
3	1	1	1	0	11	0	0	1	0
4	1	1	0	1	12	0	1	0	0
5	1	0	1	0	13	1	0	0	0
6	0	1	0	1	14	0	0	0	1
7	1	0	1	1	15	0	0	1	1
8	0	1	1	0	16	0	1	1	1

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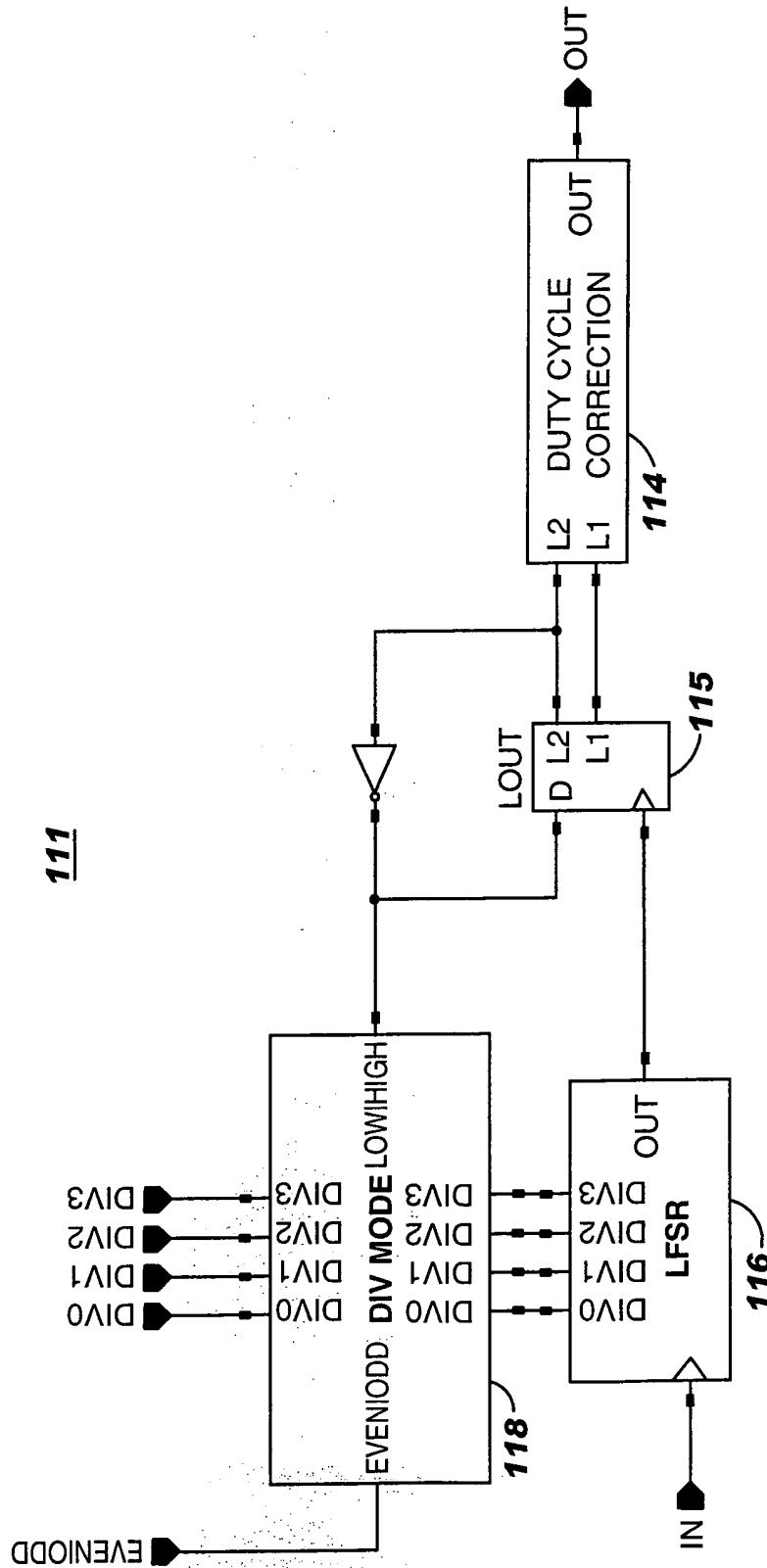
FIG. 10

110

Final Divide Value	DIV0	DIV1	DIV2	DIV3	Final Divide Value	DIV0	DIV1	DIV2	DIV3
2	0	0	0	0	18	1	1	0	0
4	1	1	1	1	20	1	0	0	1
6	1	1	1	0	22	0	0	1	0
8	1	1	0	1	24	0	1	0	0
10	1	0	1	0	26	1	0	0	0
12	0	1	0	1	28	0	0	0	1
14	1	0	1	1	305	0	0	1	1
16	0	1	1	0	32	0	1	1	1

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FIG. 11



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FIG. 12

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LFSR Divide Value	Final Divide Value	LOW HIGH=1				LOW HIGH=0			
		DIV0 'a'	DIV1 'a'	DIV2 'a'	DIV3 'a'	DIV0 'b'	DIV1 'b'	DIV2 'b'	DIV3 'b'
1	2	0	0	0	0	0	0	0	0
2,1	3	1	1	1	1	0	0	0	0
2	4	1	1	1	1	1	1	1	1
3,2	5	1	1	1	0	1	1	1	1
3	6	1	1	1	0	1	1	1	0
4,3	7	1	1	0	1	1	1	1	0
4	8	1	1	0	1	1	1	0	1
5,4	9	1	0	1	0	1	1	0	1
5	10	1	0	1	0	1	0	1	0

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FIG. 13

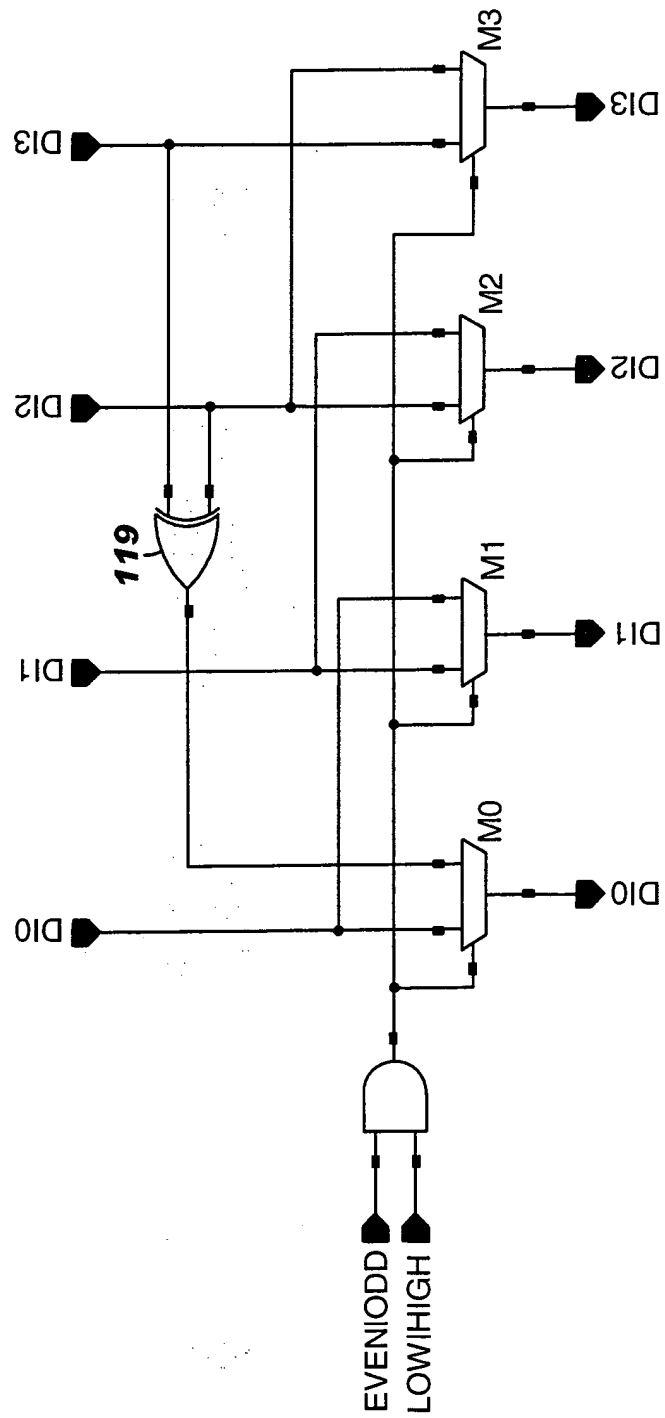
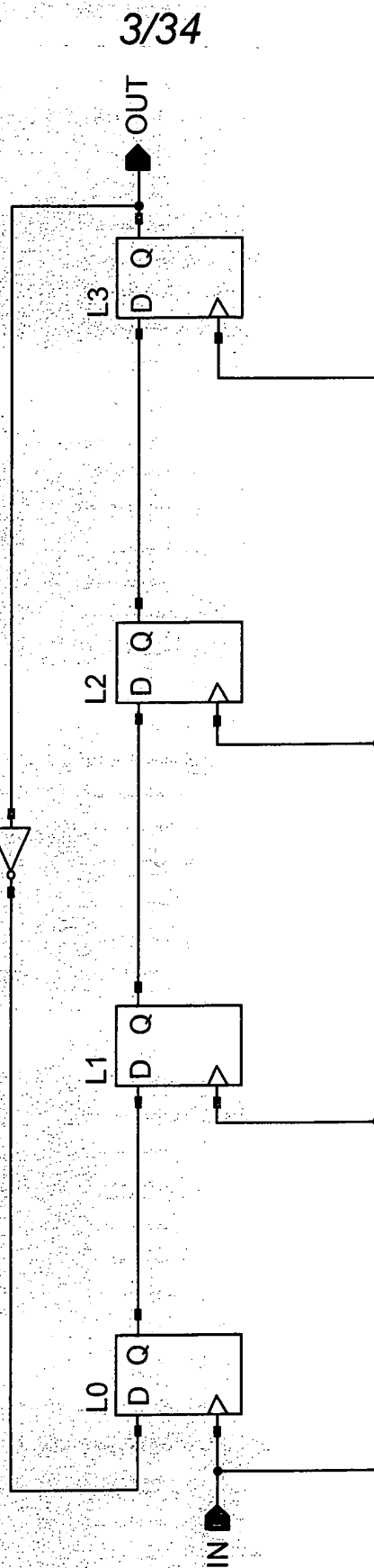
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FIG. 3
Prior Art

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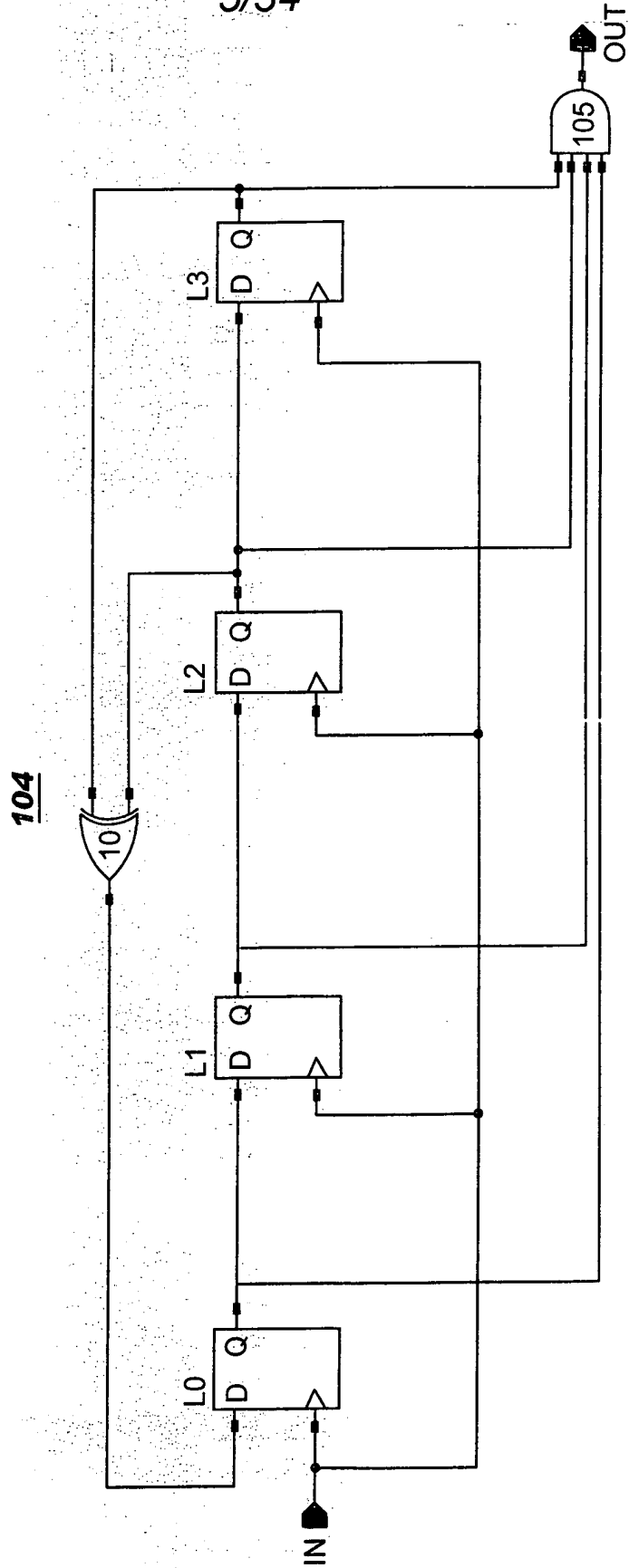
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FIG. 4
Prior Art**103**

State	L0	L1	L2	L3	State	L0	L1	L2	L3
1a	0	0	0	0	1b	0	0	1	0
2a	1	0	0	0	2b	1	0	0	1
3a	1	1	0	0	3b	0	1	0	0
4a	1	1	1	0	4b	1	0	1	0
5a	1	1	1	1	5b	1	1	0	1
6a	0	1	1	1	6b	0	1	1	0
7a	0	0	1	1	7b	1	0	1	1
8a	0	0	0	1	8b	0	1	0	1

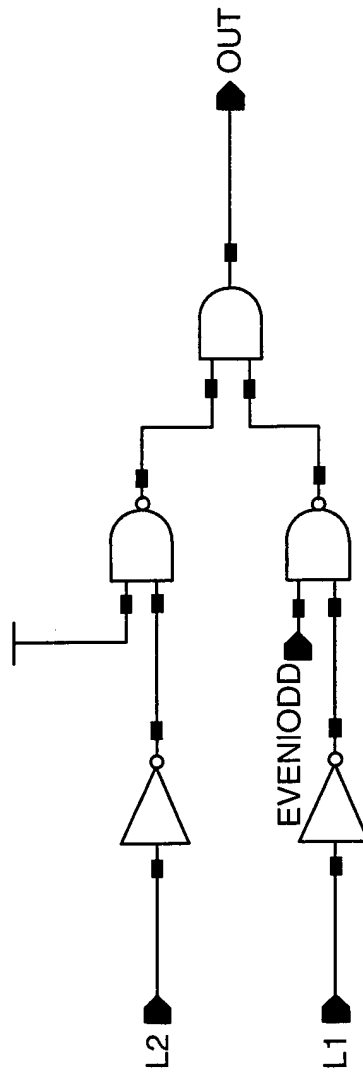
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FIG. 5
Prior Art



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FIG. 14

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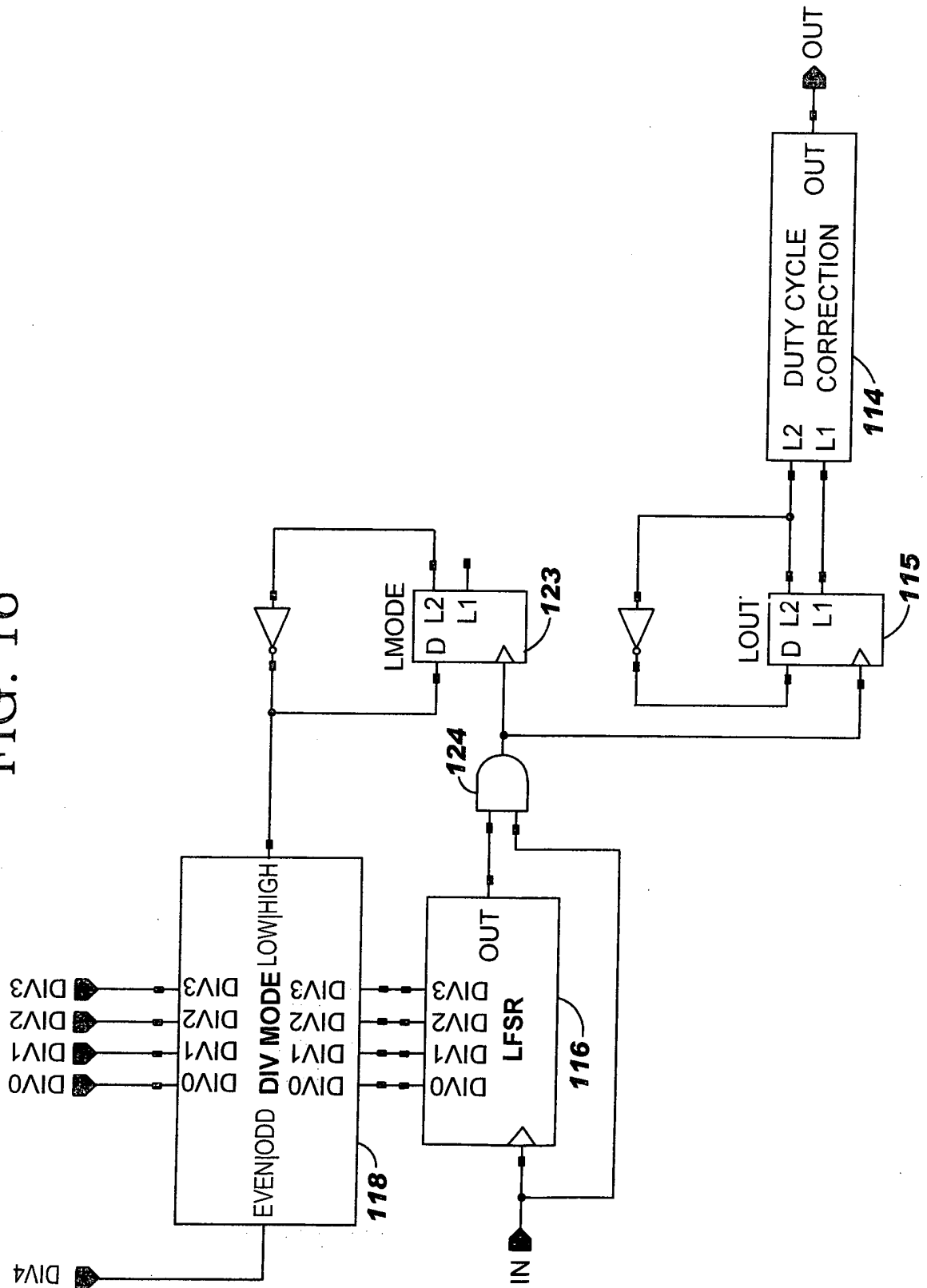
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FIG. 15

Final Divide Value	DIV0	DIV1	DIV2	DIV3	DIV4	Final Divide Value	DIV0	DIV1	DIV2	DIV3	DIV4
1	0	0	0	0	1	17	1	1	0	0	1
2	0	0	0	0	0	18	1	1	0	0	0
3	1	1	1	1	1	19	1	0	0	1	1
4	1	1	1	1	0	20	1	0	0	1	0
5	1	1	1	0	1	21	0	0	1	0	1
6	1	1	1	0	0	22	0	0	1	0	0
7	1	1	0	1	1	23	0	1	0	0	1
8	1	1	0	1	0	24	0	1	0	0	0
9	1	0	1	0	1	25	1	0	0	0	1
10	1	0	1	0	0	26	1	0	0	0	0
11	0	1	0	1	1	27	0	0	0	1	1
12	0	1	0	1	0	28	0	0	0	1	0
13	1	0	1	1	1	29	0	0	1	1	1
14	1	0	1	1	0	30	0	0	1	1	0
15	0	1	1	0	1	31	0	1	1	1	1
16	0	1	1	0	0	32	0	1	1	1	0

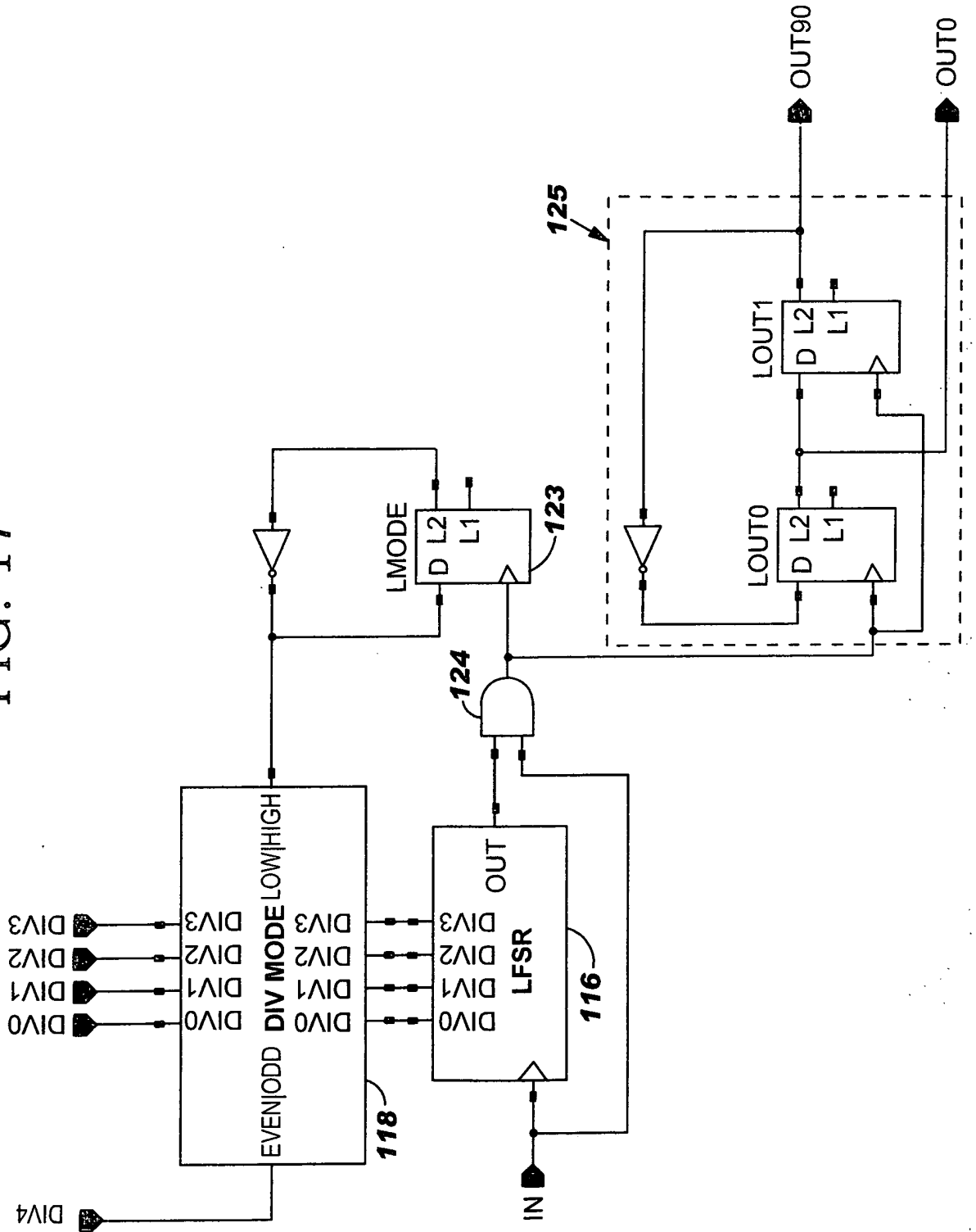
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FIG. 16



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FIG. 17



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FIG. 18

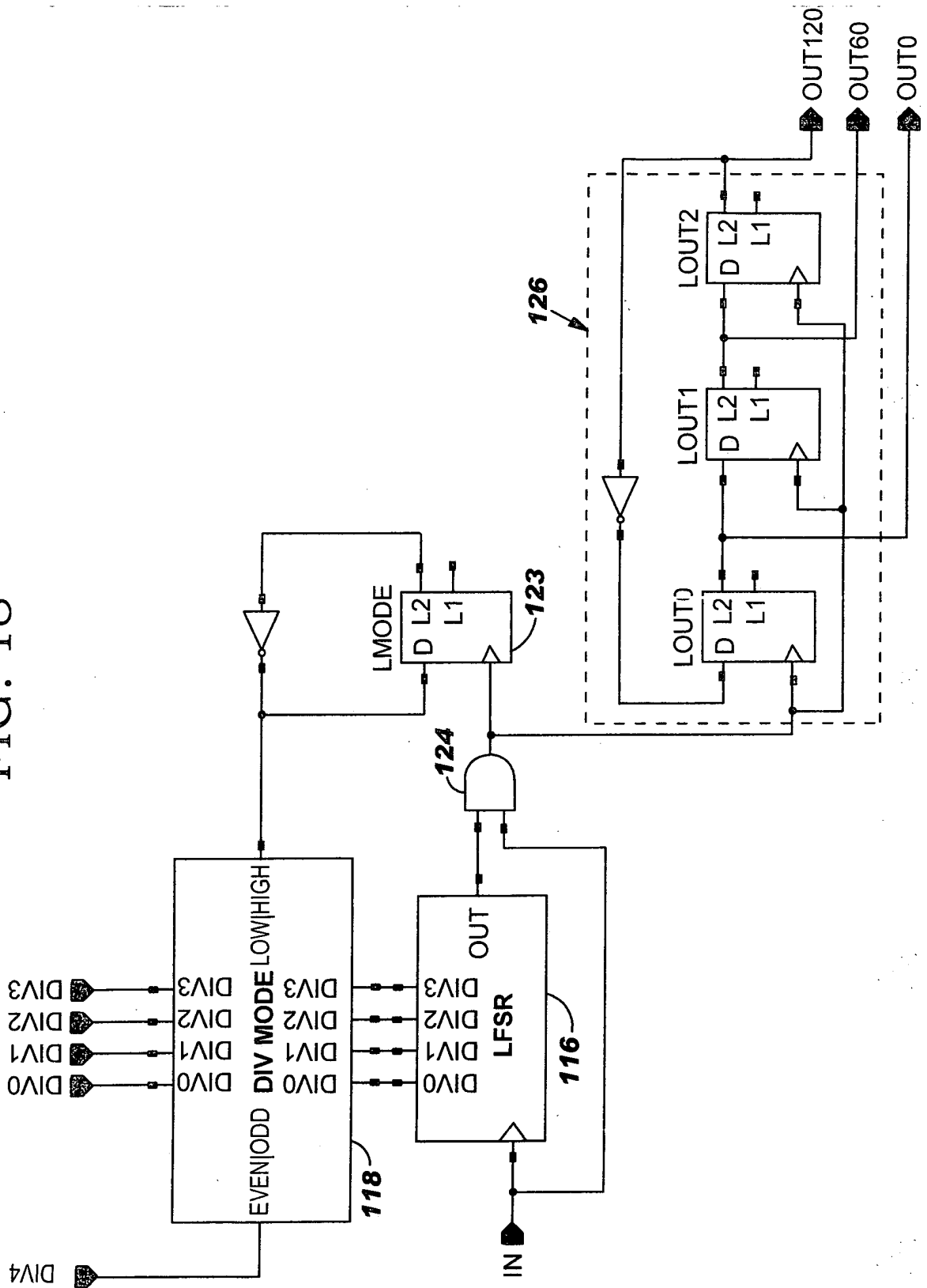
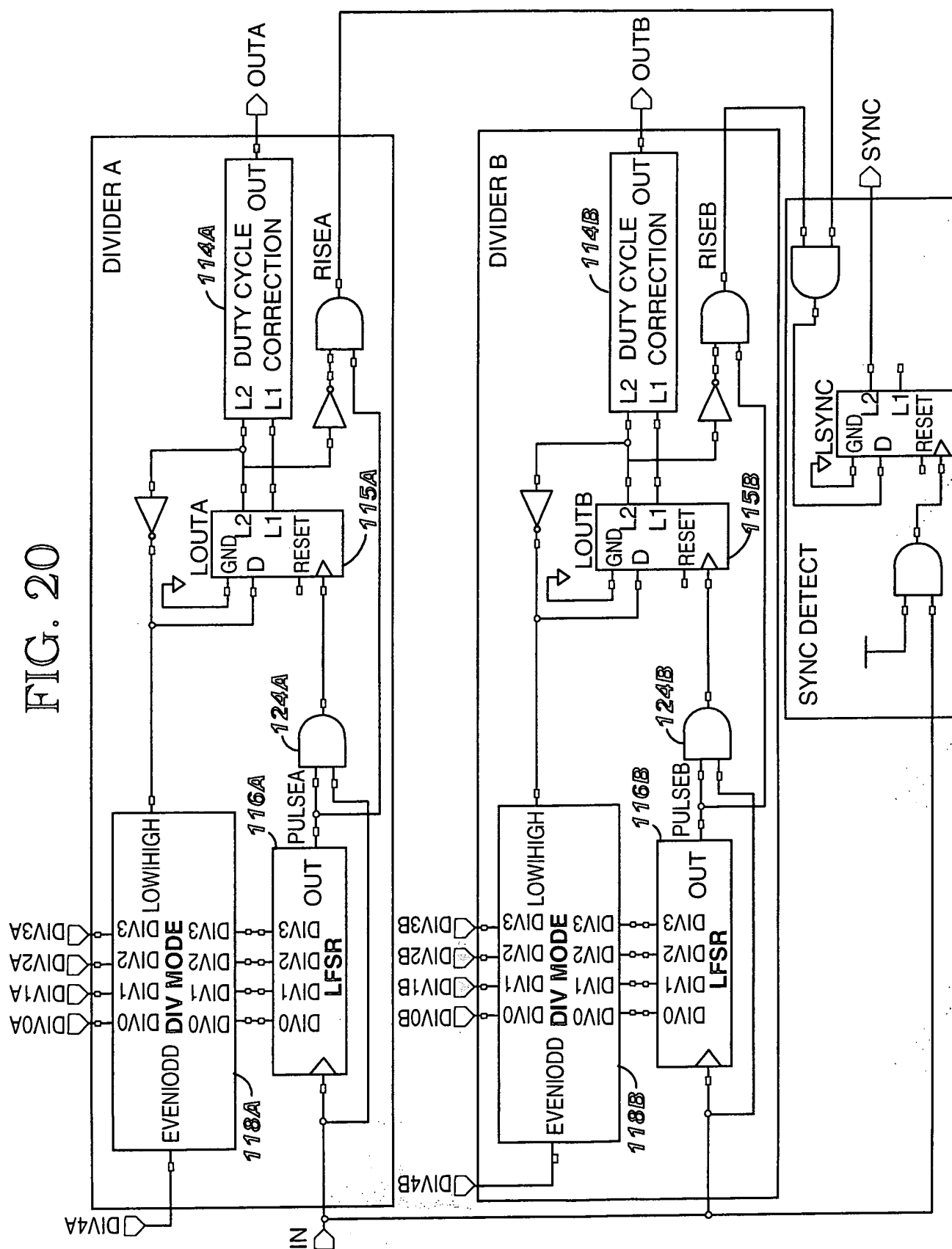
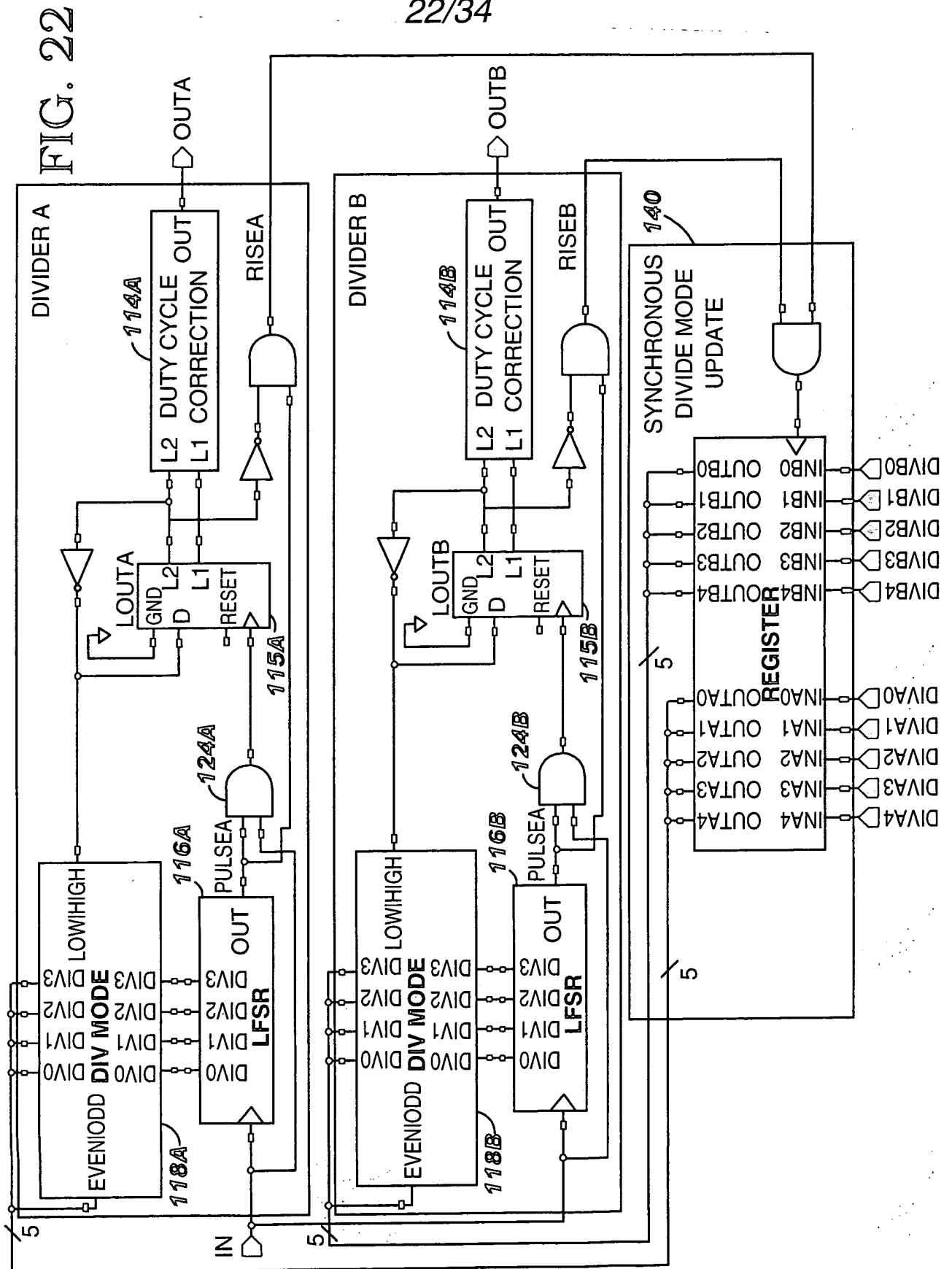


FIG. 20

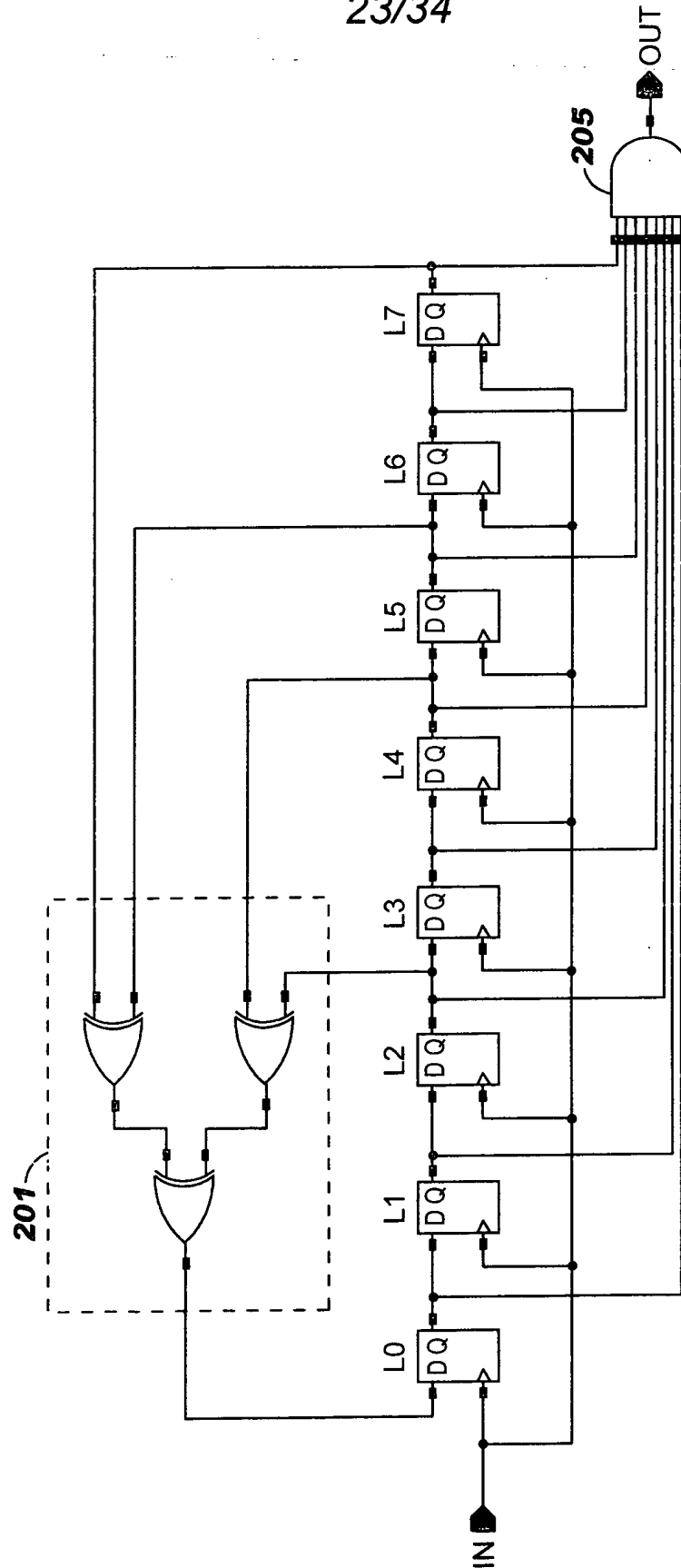


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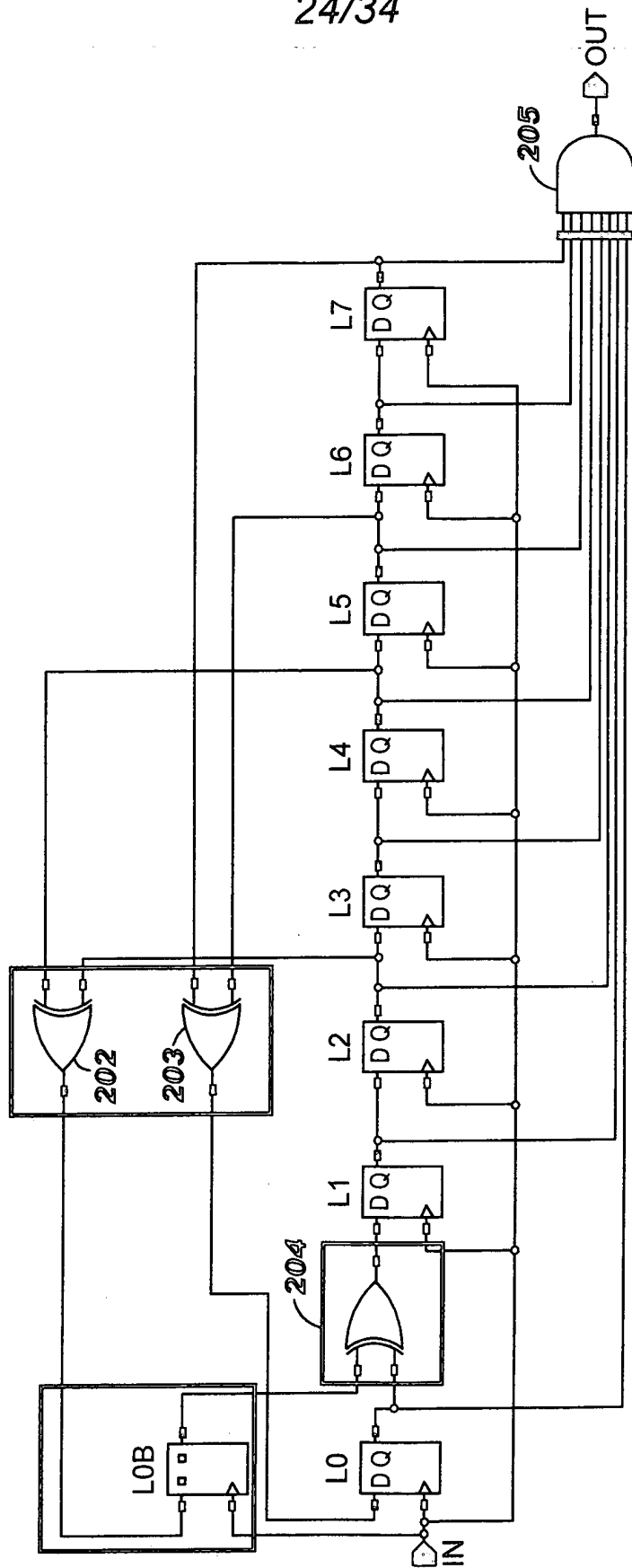
FIG. 23



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FIG. 24

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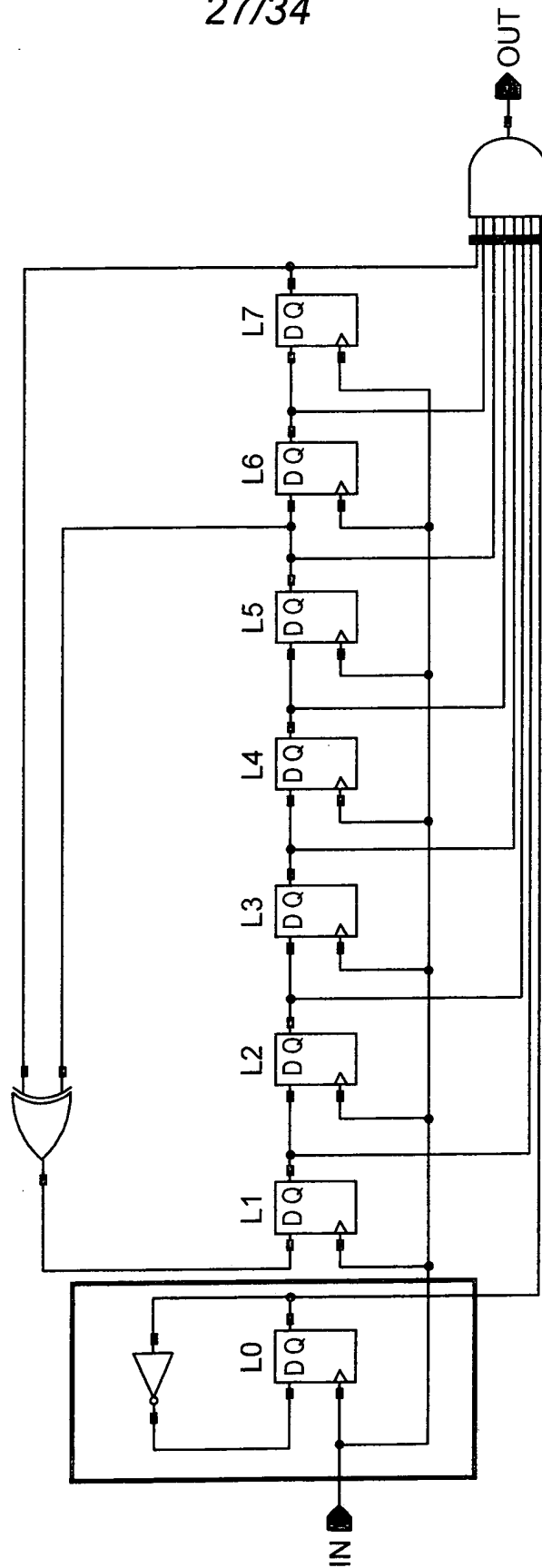
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FIG. 26

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L0	L1	L2	L3	L4	L5	L6	L7	State	Out
0	0	0	0	1	0	1	0	63	0
1	0	0	0	0	1	0	1	64	0
1	0	0	0	0	0	1	0	65	0

FIG. 27



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FIG. 28

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L0	L1	L2	State	Out
0	0	1	1	0
1	1	0	2	0
0	1	1	3	0
1	0	1	4	0
0	1	0	5	0
1	1	1	6 (2^N-2)	1
0	0	1	1	0
1	1	0	2	0
0	1	1	3	0

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FIG. 29

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L0	L1	L2	State	Out
0	0	0	1	0
1	0	1	2	0
0	1	0	3	0
1	1	1	4 [2(N-1)]	1
0	0	0	1	0
1	0	1	2	0
0	1	0	3	0

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FIG. 32

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L0	L1	L2	L3	L0B	State	Out
0	1	1	1	0	1	0
0	0	1	1	0	2	0
0	0	0	1	0	3	0
1	0	0	0	0	4	0
1	1	0	0	1	5	0
1	0	1	0	1	6	0
1	0	0	1	0	7	0
1	1	0	0	0	8	0
1	1	1	0	1	9	0
1	0	1	1	0	10	0
0	1	0	1	0	11	0
1	0	1	0	0	12	0
1	1	0	1	0	13	0
1	1	1	0	0	14	1
1	1	1	1	0	15(2 ^N -1)	0
0	1	1	1	0	1	0
0	0	1	1	0	2...	

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FIG. 33

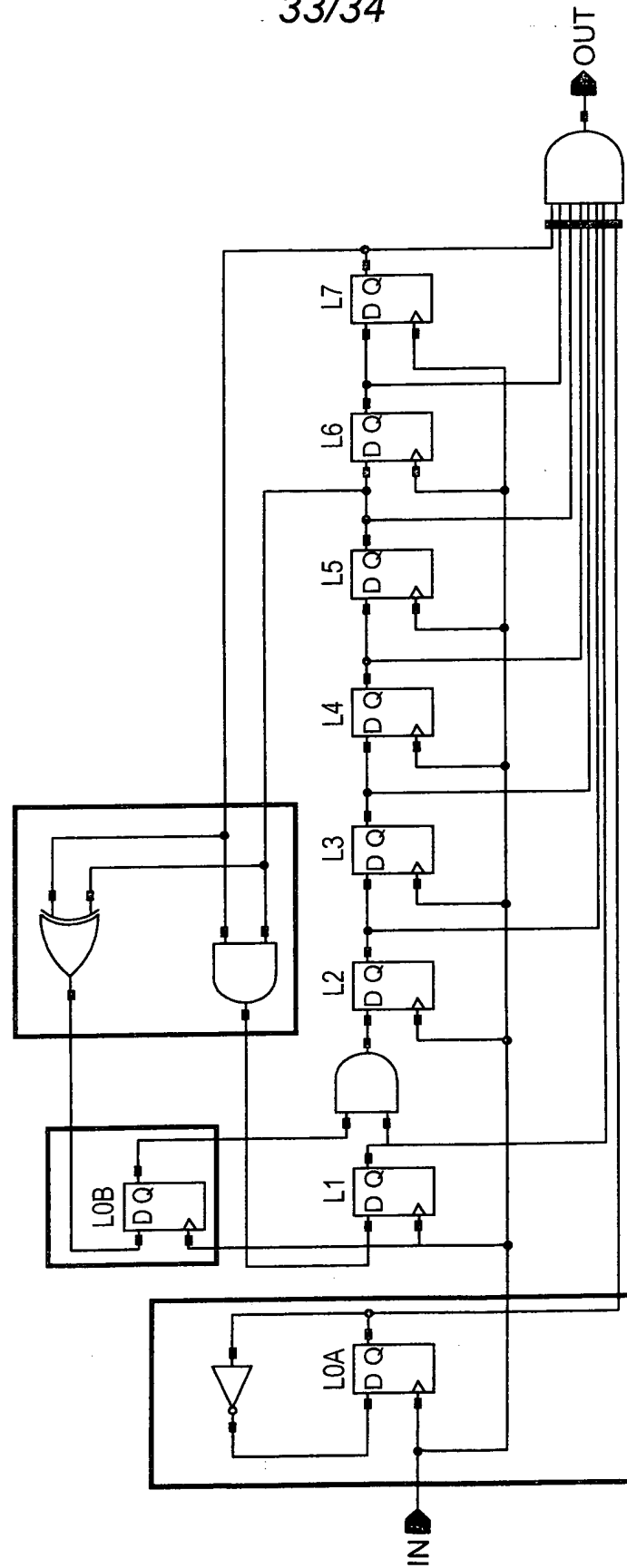


FIG. 34

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